

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.

51889/3

SERIAL NO.

10719,119

Douglas R. Hackler, Sr. et al.

FILING

November 21, 2003

GROUP

2814

U.S. PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|---------------------|-----|-----------------|----------|------------------|-------|----------|-------------------------------|
| PC | A12 | 6,104,068 | 08/15/00 | Forbes | 257 | 365 | 09/01/98 |
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| PC | A14 | 6072,354 | 06/06/00 | Tachibana et al. | 327 | 390 | 09/29/97 |
| R | A15 | 4,468,574 | 08/28/84 | Engeler et al. | 307 | 451 | 05/03/82 |
| PC | A16 | 4,300,064 | 11/10/81 | Eden | 307 | 446 | 02/12/79 |
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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.).

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EXAMINER

PHAT X. CAO

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
51889/3 USAPPLICATION NO.
10/719,119

INFORMATION DISCLOSURE CITATION

Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**

APPLICANT - Douglas R. Hackler, Sr. et al.

FILING DATE-
November 21, 2003

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|---------------------|----|--------------------|----------|----------------|-------|----------|-------------------------------|
| PC | 17 | 5,349,228 | 09/20/94 | Neudeck et al. | 257 | 365 | 12/07/93 |
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| PC | 19 | 3,755,012 | 08/28/73 | George et al. | 148 | 175 | 03/19/71 |

FOREIGN PATENT DOCUMENTS

| | | DOCUMENT NUMBER | PUBLICA- TION DATE | COUNTRY / PATENT OFFICE | CLASS | SUBCLASS | TRANSLATION | |
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| PC | 28 | Harada et al., "2-GHz RF Front-End Circuits in CMOS/SIMOX Operating at an Extremely Low Voltage of 0.5 V," IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000, pgs. 2000-2004. |
| PC | 29 | Wann et al., "CMOS with Active Well Bias for Low-Power and RF/Analog Applications," 2000 Symposium on VLSI Technology Digest of Technical Papers, 2 pgs. |
| PC | 30 | Yang et al., "Back-Gated CMOS on SOI for Dynamic Threshold Voltage Control," IEEE Transactions on Electron Devices, Vol. 44, No. 5, May 1997, pgs. 822-831. |
| PC | 31 | Assaderaghi et al., "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pgs. 414-422. |

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